PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 1/32 — A1

(11) International Publication Number: **WO 98/27482**

(43) International Publication Date: 25 June 1998 (25.06.98)

(21) International Application Number: PCT/US97/21246

(22) International Filing Date: 18 November 1997 (18.11.97)

(30) Priority Data:
08/766,089 16 December 1996 (16.12.96) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

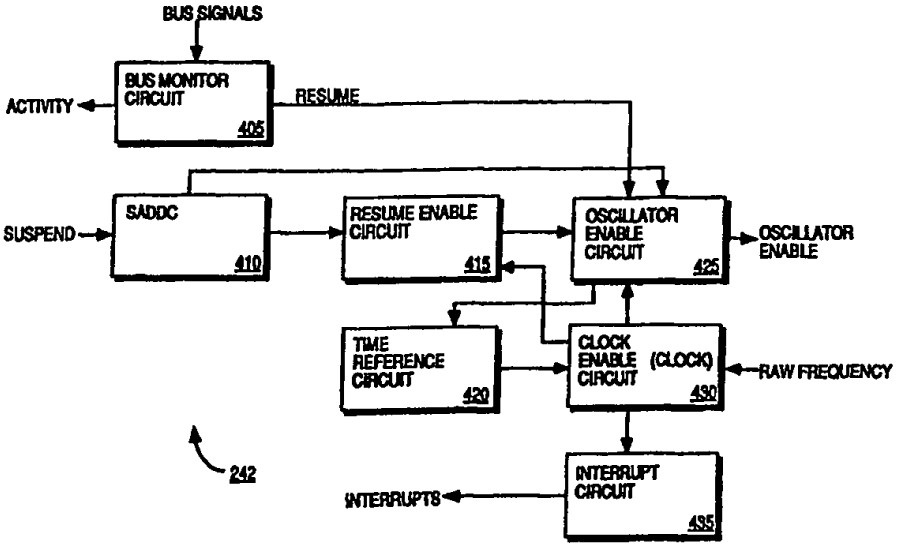
(72) Inventors: JACKSON, David, R.; 2747 N.E. Lindsey Drive, Hillsboro, OR 97124 (US). CROSS, Leonard, W.; 5043 N.W. Millstone Way, Portland, OR 97229 (US). JACOBS, Robert, A.; 2515 N.E. 40th Avenue, Portland, OR 97212 (US). OZTASKIN, Ali, S.; 15905 S.W. Falcon Drive, Beaverton, OR 97007 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD AND APPARATUS FOR SUPPORTING POWER CONSERVATION OPERATION MODES



(57) Abstract

An apparatus for managing power in an electronic device that receives the power from a bus is described. The apparatus comprises a clock enable circuit that disables a clock (430) that generates nominal clock frequencies derived from raw frequencies output by an oscillator upon receiving a first signal. A time-wise independent time reference circuit (420) is coupled to the clock enable circuit (430). The time-wise independent time reference circuit (420) sends the first signal to the clock enable circuit (430) a first predetermined period of time after receiving a signal to enter into a suspend state.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

METHOD AND APPARATUS FOR SUPPORTING POWER CONSERVATION OPERATION MODES

FIELD OF THE INVENTION

The present invention pertains to the field of power management for electronic devices. More specifically, the present invention relates to an apparatus and method for providing low power operation modes for electronic devices receiving power from a bus in a computer system.

BACKGROUND OF THE INVENTION

The Universal Serial Bus (USB) connects USB devices with a USB host. The host contains a controller which manages the operation of each USB device in the system. There is one host on each USB system. The USB physical interconnect is a tiered star topology. A hub is at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or a USB device, or a hub connected to another hub or USB device. Figure 1 illustrates the topology of the USB.

The USB transfers signals and power over a four wire cable. Two wires are designated for carrying signals from point-to-point segments. A voltage wire and a ground wire are designated in the USB cable for delivering power to USB devices. The voltage wire, VBus, is nominally 5 volts at the source. Each USB segment provides a limited amount of power over the cable. The host supplies power for use by USB devices that are directly connected. A USB host has a power management system which is independent of the USB. USB system software interacts with the host's power management system to handle system power events such as the suspend or resume modes which help with power conservation in the USB system.

The suspend mode is a power saving state which a USB device enters when the USB device sees a constant idle state on its bus lines for more than a predetermined amount of time, e.g., 3.0 milliseconds. The resume mode is

used by the host or a device to awake the USB device in the suspend state. A USB device supporting the suspend and resume mode operations must comply with a number of requirements. First, the USB device must draw less than a predetermined amount of current, presently 500 micro amps from the USB when operating in the suspend state. One approach to meeting this power constraint is achieved by powering down the clock and oscillator on the USB device when in the suspend state. Second, before powering down the clock and oscillator on the USB device, a sufficient amount of time needs to be allocated to the USB device to store current USB device state information in memory. This allows the USB device to return to the same state when it exits the suspend state. Third, when the USB device wakes-up by resume signaling, the oscillator must be given sufficient time to stabilize before enabling the clock to derive nominal frequencies from the oscillator. This prevents the clock from generating clock pulses with unstable frequencies. Fourth, sufficient time needs to be allocated to the USB device to write the stored USB device state operation into its registers before exiting the resume state and beginning normal operation.

Thus, a method and apparatus is needed for supporting power conservation modes in a device receiving power from a bus in a computer system.

SUMMARY OF THE INVENTION

According to one aspect of the invention, an apparatus for managing power in a device is described. The apparatus comprises a clock enable circuit that disables a clock that generates nominal clock frequencies derived from raw frequencies output by an oscillator upon receiving a first signal. A time-wise independent time reference circuit is coupled to the clock enable circuit. The time-wise independent time reference circuit sends the first signal to the clock enable circuit a first predetermined period of time after receiving a second signal to enter into a suspend state.

According to another aspect of the invention an apparatus for managing power in a device operating with an oscillator and a clock

deriving nominal frequencies from the oscillator is described. The apparatus comprises a bus monitoring circuit that monitors activity on a bus. The bus monitoring circuit sends an activity signal to a microcontroller on the device when activity is detected. An oscillator enable circuit is coupled to the bus monitoring circuit. The oscillator enable circuit activates the oscillator upon receiving a resume signal. A time reference circuit generates a clock enable signal a predetermined period of time after receiving the resume signal, wherein the time reference circuit operates at a time-wise independent manner relative to the oscillator and the clock. A clock enable circuit is coupled to the time reference circuit. The clock enable circuit enables the clock. The clock enable circuit disables the clock upon receiving the first signal.

According to a further aspect of the invention, a method is described for exiting a power saving mode for an electronic device powered by a bus and operating with an oscillator and a clock deriving nominal frequencies from the oscillator. According to the method, a signal to resume activity is received. The oscillator is enabled. A first predetermined period of time after the oscillator is enabled is measured, wherein the measuring is performed in a time-wise independent manner relative to the oscillator or the clock. The clock is enabled after the first predetermined period of time.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 illustrates the topology of the Universal Serial Bus;

Figure 2 illustrates a block diagram of a computer system implementing one embodiment of the present invention;

Figure 3 illustrates a block diagram of an embodiment of a Universal Serial Bus device implementing the present invention;

Figure 4 illustrates a block diagram of an embodiment of the suspend control circuit according to one embodiment of the present invention;

Figure 5 is one embodiment of an R-C network used in the present invention;

Figure 6 is diagram illustrating the frequencies generated by an oscillator over time and clock pulses derived from the oscillator frequencies;

Figure 7 is a timing diagram illustrating the signals in the suspend control circuit; and

Figure 8 is a flow chart illustrating a method for supporting power conservation modes in an electronic device receiving power from a bus.

DETAILED DESCRIPTION

Referring to Figure 2, an exemplary computer system upon which an embodiment of the present invention can be implemented is shown as 200. The computer system 200 comprises a processor 201 that processes digital data. The processor 201 can be a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a processor implementing a combination of instruction sets, or other processor device. The processor 201 is coupled to a CPU bus 210 which transmits signals between the processor 201 and other components in the computer system 200.

For the illustrated embodiment, a memory 213 comprises a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, or other memory devices. The memory 213 stores information or other intermediate data during execution by the processor 201. A bridge memory controller 211 is coupled to the CPU bus 210 and the memory 213. The bridge memory controller 111 directs data traffic between the processor 201, the memory 213, and other components in the computer system 200 and bridges signals from these components to a high speed I/O bus 220.

For the illustrated embodiment, the high speed I/O bus 220 supports peripherals operating at high data throughput rates. The bus 220 can be a single bus or a combination of multiple buses. As an example, the bus 220 can comprise a Peripheral Components Interconnect (PCI) bus, a Personal

Computer Memory Card International Association (PCMCIA) bus, or other buses. The bus 220 provides communication links between components in the computer system 200. A network controller 221 links a network of computers together and provides communication among the machines. A display device controller 222 is coupled to the high speed I/O bus 220. The display device controller 222 allows coupling of a display device to the computer system and acts as an interface between the display device and the computer system 200. The display device receives information and data from the processor 201 through the display device controller 222 and displays the information and data to the user of the computer system 200.

In the illustrated embodiment, a bus bridge 223 couples the high speed I/O bus 220 to I/O bus 230 and I/O bus 240. The bus bridge 223 comprises a translator to bridge signals between the high speed I/O bus 220 and the I/O bus 230 and the I/O bus 240.

The I/O bus 230 is used for communicating information between peripheral device which operate at lower throughput rates. The I/O bus 230 can be a single bus or a combination of multiple buses. As an example, the bus 230 can comprise an Industry Standard Architecture (ISA) bus, an Extended Industry Standard Architecture (EISA) bus or a Micro Channel Architecture (MCA) bus. The bus 230 provides communication links between components in the computer system 200. A data storage device 231 can be a hard disk drive, a floppy disk drive, a CD-ROM device, a flash memory device or other mass storage device.

I/O bus 240 is a bus having the capability to power devices coupled to it. The I/O bus 240 can be a single bus or a combination of multiple buses. In one embodiment of the computer system 200, the I/O bus 240 is a USB and bus bridge 223 operate as a host controller to the USB 240. The bus 240 provides communication links between components in the computer system. Component 241 is a USB device coupled to bus 240. The USB device 241 may be for example a video camera, audio speakers, a keyboard controller, an audio controller, or other devices. Suspend control circuit 242 resides

inside USB device 241 and operates to support power conservation modes for the USB device 241. It should be appreciated that suspend control circuit 242 may be implemented in devices other than USB devices receiving power from buses other than the USB.

Figure 3 is a block diagram of an embodiment of a USB device 241 implementing the present invention. USB device 241 includes a microcontroller circuit 301 that operates to process information and support functions on the USB device 241. A suspend control circuit 242 is coupled to the microcontroller circuit 301. The suspend control circuit 242 operates to support a low power operation mode in the USB device 241. Oscillator unit 302 is coupled to suspend control circuit 242. Oscillator unit 302 operates to provide clocking at a raw frequency to the USB device 241. Oscillator unit 302 includes an oscillator that generates wave forms and a cell that derives clock pulses from the oscillator wave forms. A raw frequency is a frequency generated directly by the oscillator unit 302. Nominal or sub-frequencies are derived from the raw frequency by a clock in the suspend control circuit 242.

The suspend control circuit 242 monitors activity on the USB 240 by detecting a non-idle condition on the USB 240. Suspend control circuit 242 sends an activity signal to microcontroller circuit 301 when the suspend control circuit 242 detects activity on the USB 240. The microcontroller 301 defines a window of time in which it waits for the activity signal from the suspend control circuit 242. If the microcontroller 301 does not receive an activity signal during the window of time, it sends a suspend signal to the suspend control circuit 242 indicating that the USB device 241 should be put into a suspend state. When operating in the suspend state, the USB device 241 reduces its power consumption by disabling the clock in suspend control circuit 242 and oscillator unit 302 in the USB device 241. Disabling the clock in suspend control circuit 242 and oscillator unit 302 puts the USB device 241 in a static state where current consumption comes only from current leakage from the components in the USB device 241.

Suspend control circuit 242 provides a delay to allow USB device state information to be stored before disabling its own clock and oscillator unit 302. Upon receiving the suspend signal from the microcontroller 301, the suspend control circuit 242 activates a time reference circuit residing inside the suspend control circuit 242. After a predetermined period of time, the time reference circuit signals the suspend control circuit 242 to disable the clock and external oscillator unit 302. The time reference circuit is configured to provide an adequate period of time for microcontroller 301 to store state information of the USB device 241 into a memory before disabling the clock and oscillator unit 302. The time reference circuit is time-wise independent of the clock and the oscillator unit 302 in the USB device 241. After the microcontroller 301 has stored the USB device state information in memory, the suspend control circuit 242 disables the clock residing in the suspend control circuit 242. After the clock residing in the suspend control circuit 242 has been disabled, the suspend control circuit 242 disables the oscillator unit 302.

Suspend control circuit 242 continues to monitor the USB 240 while device 241 is in the suspend mode. When activity is detected on the USB 240, the suspend control circuit 242 enters into a resume state. Upon entering the resume state, suspend control circuit 242 enables the oscillator unit 302. Suspend control circuit 242 allows an adequate period of time for the oscillator unit 302 to stabilize before enabling the clock inside suspend control circuit 242. The period of time is measured by the time reference circuit residing in suspend control circuit 242. The time reference circuit is time-wise independent of the clock and the oscillator unit 302 in the USB device 241 and thus provides a reliable timing reference because it does not require time to stabilize. After both the oscillator unit 302 and the clock are enabled, suspend control circuit 242 sends an interrupt signal to microcontroller 301 indicating to microcontroller 301 that resume mode has started and to update the registers in the microcontroller 301 with USB state information stored in memory. After the registers have been updated,

suspend control circuit 242 sends a second interrupt signal to microcontroller 301 indicating that the resume mode has ended and to begin normal activity. Microcontroller 301, suspend control circuit 242, and oscillator unit 302 may be implemented by any known circuitry.

Figure 4 illustrates a block diagram of an embodiment of the suspend control circuit 242 according to one embodiment of the present invention. Suspend control circuit 242 includes a bus monitor circuit 405. Bus monitor circuit 405 operates to monitor activity on the USB 240 by detecting bus signals on the USB 240. Bus monitoring circuit 405 generates an activity signal or an activity bit when the bus monitoring circuit 405 detects activity on the USB 240. The activity signal is sent to a microcontroller and used by the microcontroller to determine whether or not to put the USB device 241 into a suspend state. When the USB device 241 is in the suspend state, it draws less than a predetermined amount of current, 500 micro amps for the illustrated embodiment, from the USB. This reduction of power consumption is achieved by disabling the clock of suspend control circuit 242 (which for the illustrated embodiment is disposed inside clock enable circuit 430) and the oscillator unit 302 in the USB device. The activity signal is also sent to an oscillator enable circuit 425 which passes a signal to the time reference circuit 420.

Suspend control circuit 242 further includes a suspend assert/deassert detect circuit (SADDC) 410. The SADDC 410 is coupled to the microcontroller 301 and receives a suspend signal from the microcontroller 301 when the microcontroller 301 determines that the USB device 241 should enter the suspend state. The SADDC 410 first drives a signal to the resume enable circuit 415 to block bus activity from prematurely halting the suspend process. The resume enable circuit 415 drives a signal to the oscillator enable circuit 425 indicating that the USB device 241 is to enter the suspend state. The oscillator enable circuit 425 then passes a signal to the time reference circuit 420.

The time reference circuit 420 receives the signal indicating that the USB device 241 is to enter the suspend state from the oscillator enable circuit 410 and provides a delay before disabling the clock in the clock enable circuit 430. The delay allows the microcontroller 301 to store USB device state information into a local memory before the microcontroller 301 enters the suspend mode. In one embodiment of the present invention, the time reference circuit 420 comprises a delay circuit using a resistive-capacitive (R-C) network operating independently time-wise of the clock and oscillator unit 302 on the USB device 241. The resistor and capacitor in the R-C network are configured to provide a delay adequate for allowing the microcontroller to store USB device state information into the memory. The amount of delay required is application dependent and empirically determined.

Figure 5 illustrates one embodiment of an R-C network 500 used in the present invention. The diode 510 is coupled to a supply voltage of the USB device. When no power is applied to the R-C network 500, Vcc and ground are at the same potential and the capacitor 520 is able to discharge through the diode 510. An rc_out signal is used to provide voltage for the capacitor 520 in the R-C network to charge. The rc_in signal is monitored to determine whether the circuit has been charged up. The amount of time to charge up the R-C network is dependent on the values used for the resistor and capacitor components which, as described earlier, are applicant dependent and empirically determined. The R-C network may be used to measure a period of time in both direction whether it is being charged or discharged. After the delay, the time reference circuit 420 drives a signal to the clock enable circuit 430 to indicate that the microcontroller has had time to store USB device state information in memory.

Referring back to Figure 4, the clock enable circuit 430 includes a clock that derives nominal or sub-frequencies from an oscillator unit 302 external to the suspend control logic 242. The clock enable circuit 430 disables the clock upon receiving a signal from the time reference circuit 420 indicating that the microcontroller has completed storing USB device state

information. After a predetermined period of time measured by using the oscillator unit as a reference, clock enable circuit 430 signals oscillator enable circuit 425 to disable the oscillator unit 302. The clock in the clock enable circuit 430 is disabled before disabling the oscillator unit 302. Disabling the clock first prevents the clock from deriving an unstable clock signal from an unstable output of the oscillator unit 302. An unstable clock signal may cause the microcontroller to be put in an invalid state. In one embodiment of the present invention, the predetermined period of time is measured by the raw frequency generated by the oscillator unit 302 and the predetermined period of time is one period defined by the oscillator unit 302.

During the suspend state, bus monitor circuit 405 continues to monitor the activities on the USB 240. Upon detecting activity on the USB 240, bus monitor circuit 405 drives a resume signal to the oscillator enable circuit 425 and the oscillator enable circuit 425 then sends a signal to the time reference circuit 420. The oscillator enable circuit 425 enables the oscillator unit 302 upon receiving the resume signal from the bus monitor circuit 405. The time reference circuit 420 provides a predetermined delay before driving a signal to the clock enable circuit 430 that enables the clock upon receiving the resume signal from the bus monitor circuit 405. The predetermined delay allows the oscillator unit to stabilize before allowing the clock in clock enable circuit 430 to derive nominal or sub-frequencies from the raw frequencies output by oscillator unit 302.

Figure 6 is a diagram illustrating an example of the raw clock frequencies output from an oscillator of oscillator unit 302 over a period of time. Wave form 610 is the output generated from the oscillator. The waves generated by the oscillator from time 0 to time t have amplitude that fluctuate in magnitude. After a time t, the oscillator stabilizes and produces waves having amplitudes that do not fluctuate. Pulse form 620 is the output of a cell of oscillator unit 302 deriving raw frequencies from the wave output of the oscillator. The waves with fluctuating amplitudes generated by the oscillator from time 0 to time t causes the cell to generate imperfect raw frequencies that

have unstable frequencies at time 0 to time t. Raw frequencies generated after time t from the waves having amplitudes that do not fluctuate have stable frequencies.

Referring back to Figure 4, as described earlier, the clock in clock enable circuit 430 is enabled after the oscillator unit 302 has stabilized. Time reference circuit 420 provides a predetermined delay after the oscillator unit 302 has been enabled giving the oscillator unit 302 time to stabilize before enabling the clock in clock enable circuit 430. In one embodiment of the present invention, the time reference circuit 420 utilizes the same R-C network described above for providing the predetermined delay. In an alternate embodiment of the present invention, a different R-C network with a different configuration but still operating in a time-wise independent manner relative to the clock or the oscillator unit 302 is used. The resistor and capacitor in the R-C network are configured to provide a delay adequate for allowing the oscillator unit 302 to stabilize before enabling the clock to derive nominal or sub-frequencies from the raw frequencies output by the oscillator unit 302. Similarly, the amount of delay required is application dependent and empirically determined.

An interrupt circuit 435 is coupled to the clock enable circuit 430 and the microcontroller shown in Figure 3. After the clock in the clock enable circuit 430 has been enabled, the clock enable circuit 430 drives a resume start signal to the interrupt circuit 435. In response to the resume start signal, interrupt circuit 435 drives a first interrupt to the microcontroller 301. The first interrupt indicates to the microcontroller 301 that the resume state has started and that the USB device state information stored in memory during suspend mode must be written back into the registers in the microcontroller 301. After the USB device 241 state information has been restored back into the registers of the microcontroller 301, the interrupt circuit 435 drives a second interrupt signal to the microcontroller 301, indicating that the resume state has ended and that the USB device 241 is back in a normal operation state. The USB signals the end of resume when both of its lines are driven

low for a period of time. The bus monitor circuit 405 sees this condition and drives this second interrupt to the microcontroller 301.

In one embodiment of the present invention, a resume enable circuit 415 is coupled to the SADDC 410, oscillator enable circuit 425, and clock enable circuit 430. Resume enable circuit 415 operates to allow the USB device 241 to complete the steps of entering into the suspend state before allowing the USB device 241 to begin steps for entering into the resume state. SADDC 410 sends a signal to the time reference circuit 420 indicating that the USB device 241 is to enter the suspend state, by way of the resume enable circuit 415. The resume enable circuit 415 drives a signal to oscillator enable circuit 425 and on through to the time reference circuit 420 causing any resume signals from the bus monitoring circuit 405 to be blocked from the oscillator enable circuit 425 and consequently blocked from the time reference circuit 420 also. This allows the USB device 241 to complete the steps for entering into the suspend state without interruption. Once the clock enable circuit 430 receives a signal from the time reference circuit 420, indicating that the microcontroller 301 has completed storing USB state information and is about to enter into the suspend state, the clock enable circuit 430 drives a signal to the resume enable circuit 415. In response, the resume enable circuit 415 drives a signal to the oscillator enable circuit 425 that removes the blocking of the resume signal from the bus monitor circuit 405. In one embodiment of the present invention, the bus monitor circuit 405, SADDC 410, resume enable circuit 415, time reference circuit 420, oscillator enable circuit 425, clock enable circuit 430, and interrupt circuit 435 all reside on a single chip on the same silicon substrate.

The bus monitor circuit 405, SADDC 410, resume enable circuit 415, time reference circuit 420, oscillator enable circuit 425, clock enable circuit 430, and interrupt circuit 435 may be implemented by any known circuitry. It should be appreciated that the suspend control circuit 242 illustrated in Figure 4 may be implemented in devices other than USB devices that receive power from buses other than the USB.

Figure 7 is a timing diagram illustrating the signals in the suspend control circuit. At time 0, the USB device is operating in a normal operation state. At time 5, suspend is detected. The microcontroller sends a suspend pulse to the suspend control circuit after a period of inactivity on the USB. A suspend assert/deassert detect circuit in the suspend control circuit receives the suspend pulse and drives a signal to a time reference circuit in the suspend control circuit. The time reference circuit asserts a signal shown as rc_out through a delay circuit. At time 10, the delay circuit responds by asserting a signal on rc_in. The time period between the assertion of rc_out and rc_in is used by the microcontroller to store USB device state information into memory.

At time 15 activity directed to the USB device is detected by the bus monitoring circuit. Bus monitoring circuit in the suspend control circuit sends a resume pulse to the oscillator enable circuit and time reference circuit by way of oscillator enable circuit. The time reference circuit deasserts the signal shown as rc_out. At time 20, the delay circuit responds by de-asserting a signal on rc_in. The independent time period between the de-assertion of rc_out and rc_in is used as a reference by the clock enable circuit in the suspend control circuit. The clock enable circuit uses this time period as a reference to allow the oscillator unit to stabilize before enabling its clock.

At time 20, a resume start interrupt signal is sent to the microcontroller by an interrupt circuit after the clock has been enabled. The microcontroller responds to the resume start interrupt by writing the USB device state information stored in memory into the registers of the microcontroller. At time 25, a resume end interrupt is sent by the interrupt circuit to the microcontroller. The resume end interrupt informs the microcontroller that the USB device will be running in normal operation mode.

Figure 8 is a flow chart illustrating a method of exiting a power saving mode for an electronic device powered by a bus. The electronic device operates with an oscillator and a clock deriving a nominal frequency

from the oscillator. At step 801, it is determined whether there is activity on the bus directed to the electronic device. If there is no activity on the bus directed to the electronic device, control proceeds to step 801. If there is activity on the bus directed to the electronic device, control proceeds to step 802.

At step 802, the oscillator is enabled.

At step 803, a period of time is independently measured from the time the oscillator is enabled. The measuring is performed by using a time reference that is independent of the oscillator and the clock. In one embodiment of the present invention, the independent measurement is achieved by sending a signal through a delay circuit. The delay circuit could be implemented by using a resistive-capacitive network. The period of time is greater than the time required for the oscillator to stabilize.

At step 804, the clock is enabled after the period of time has expired.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than an restrictive sense.

CLAIMS

What is claimed is:

1. An apparatus for managing power in a device comprising:

a clock enable circuit that disables a clock that generates nominal clock frequencies derived from an oscillator upon receiving a first signal; and

a time reference circuit, coupled to the clock enable circuit, that sends the first signal to the clock enable circuit a first predetermined period of time after receiving a second signal indicating that the device is to enter a suspend state, wherein the time reference circuit operates in a time-wise independent manner relative to the oscillator and the clock.

2. The apparatus of Claim 1, wherein the time reference circuit comprises a resistor-capacitor network that operates in a time-wise independent manner relative to the oscillator.

3. The apparatus of Claim 1, further comprising an oscillator enable circuit, coupled to the clock enable circuit, that disables the oscillator upon receiving a third signal to disable the oscillator.

4. The apparatus of Claim 3, wherein the clock enable circuit sends the third signal to disable the oscillator to the oscillator enable circuit a second predetermined period of time after receiving the first signal.

5. The apparatus of Claim 3, wherein the oscillator enable circuit enables the oscillator upon receiving a resume signal.

6. The apparatus of Claim 5, wherein the clock enable circuit enables the clock to generate the nominal clock frequencies derived from the oscillator upon receiving a fourth signal.

7. The apparatus of Claim 6, wherein the time reference circuit sends the fourth signal to the clock enable circuit a third predetermined period of time after receiving the resume signal.

8. An apparatus for managing power in a device operating with an oscillator and a clock deriving nominal frequencies from the oscillator, comprising:

a suspend control circuit that receives a suspend signal from a microcontroller after a period a predetermined amount of inactivity is detected;

an oscillator enable circuit, coupled to the suspend control circuit, that receives the suspend signal from the suspend control circuit;

a clock enable circuit that disables the clock upon receiving a first signal; and

a time reference circuit, coupled to the oscillator enable circuit and the clock enable circuit, that sends the first signal to the clock enable circuit a first predetermined period of time after receiving a second signal indicating that the device is to enter a suspend state from the oscillator enable circuit, wherein the time reference circuit operates in a time-wise independent manner relative to the oscillator and the clock.

9. The apparatus of Claim 8, wherein the time reference circuit is a resistor-capacitor network.

10. The apparatus of Claim 8, further comprising an oscillator enable circuit, coupled to the clock enable circuit, that disables the oscillator upon receiving a third signal to disable the oscillator.

11. The apparatus of Claim 10, wherein the clock enable circuit sends the oscillator disable signal to the oscillator enable circuit a second predetermined period of time after receiving the first signal.

12. The apparatus of Claim 10, wherein the oscillator enable circuit enables the oscillator upon receiving a resume signal from the microcontroller.

13. The apparatus of Claim 10, wherein the clock enable circuit enables the clock to generate the nominal clock frequencies derived from the oscillator upon receiving a fourth signal.

14. The apparatus of Claim 13, wherein the time reference circuit sends the fourth signal to the clock enable circuit a third predetermined period of time after receiving the resume signal.

15. The apparatus of Claim 13, further comprising an interrupt circuit, coupled to the clock enable circuit, that generates a first interrupt signal to the microcontroller that signals the microcontroller to configure the electronic device for operation upon receiving the fourth signal from the clock enable circuit.

16. The apparatus of Claim 15, wherein the interrupt circuit generates a second interrupt signal to the microcontroller that signals the microcontroller that the electronic device is in operation a fourth predetermined period of time after receiving the second signal.

17. An apparatus for managing power in a device operating with an oscillator and a clock deriving nominal frequencies from the oscillator, comprising:

a bus monitoring circuit that monitors activity on a bus and that generates a resume signal when activity is detected;

an oscillator enable circuit, coupled to the bus monitoring circuit, that activates the oscillator upon receiving the resume signal;

a time reference circuit, coupled to the oscillator enable circuit, that generates a clock enable signal a predetermined period of time after receiving the resume signal, wherein the time reference circuit operates in a time-wise independent manner relative to the oscillator and the clock; and

a clock enable circuit, coupled to the time reference circuit, that enables the clock after receiving the clock enable signal.

18. The apparatus of Claim 17, wherein the time reference circuit comprises a resistive-capacitive network.

19. A method for managing power in an electronic device receiving the power from a bus and operating with an oscillator and a clock deriving nominal frequencies from the oscillator, comprising:

monitoring activity on the bus;

entering suspend mode after a predetermined period of inactivity has been detected;

storing state information of the device in memory;

disabling the clock after a first predetermined period of time after entering suspend mode; and

disabling the oscillator a second predetermined period of time after the clock has been disabled.

20. The method of Claim 19, further comprising the steps of:

entering resume mode after activity is detected on the bus;

enabling the oscillator;

enabling the clock a third predetermined period of time after the oscillator has been enabled; and

updating the device with the state information in the memory.

21. The method of Claim 20, wherein the third predetermined period of time is measured by sending a signal through an independent clock reference circuit.

22. A method of exiting a power saving mode for an electronic device powered by a bus and operating with an oscillator and a clock deriving nominal frequencies from the oscillator, comprising:

receiving a signal to resume activity;

enabling the oscillator;

measuring a first predetermined period of time after the oscillator is enabled, wherein the measuring is performed independent of using the oscillator or the clock; and

enabling the clock after the first predetermined period of time.

23. The method of Claim 22, wherein the measuring step is performed by sending a signal through a resistive-capacitive network having a time constant.

Fig. 1

(PRIOR ART)

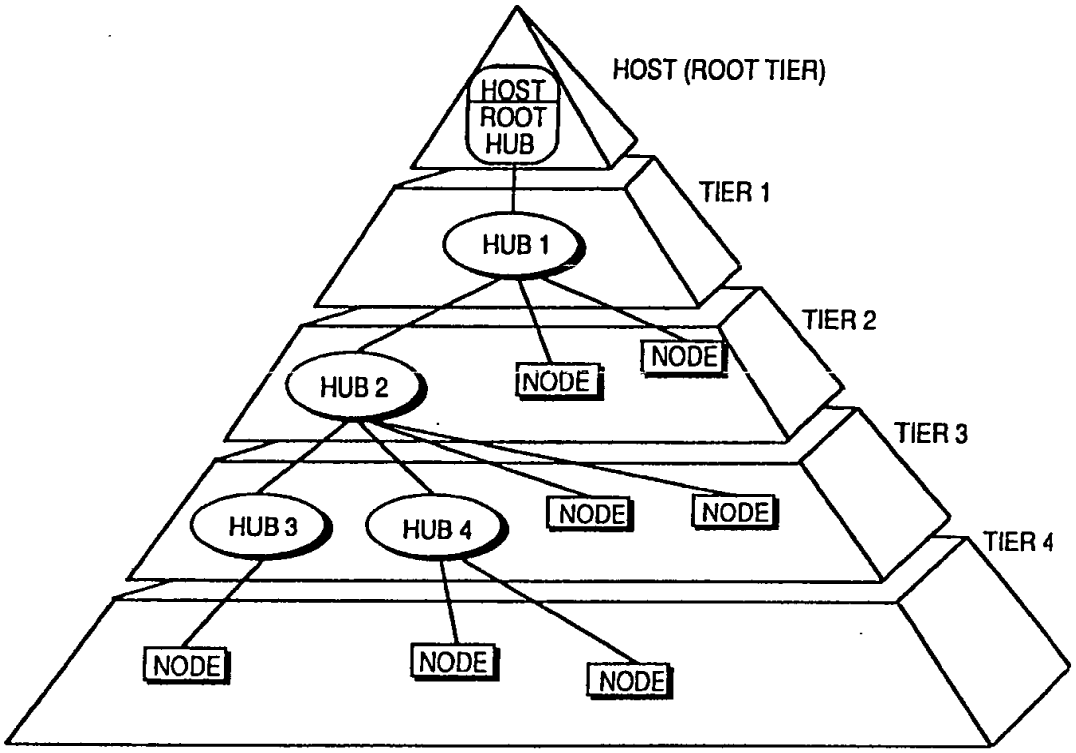
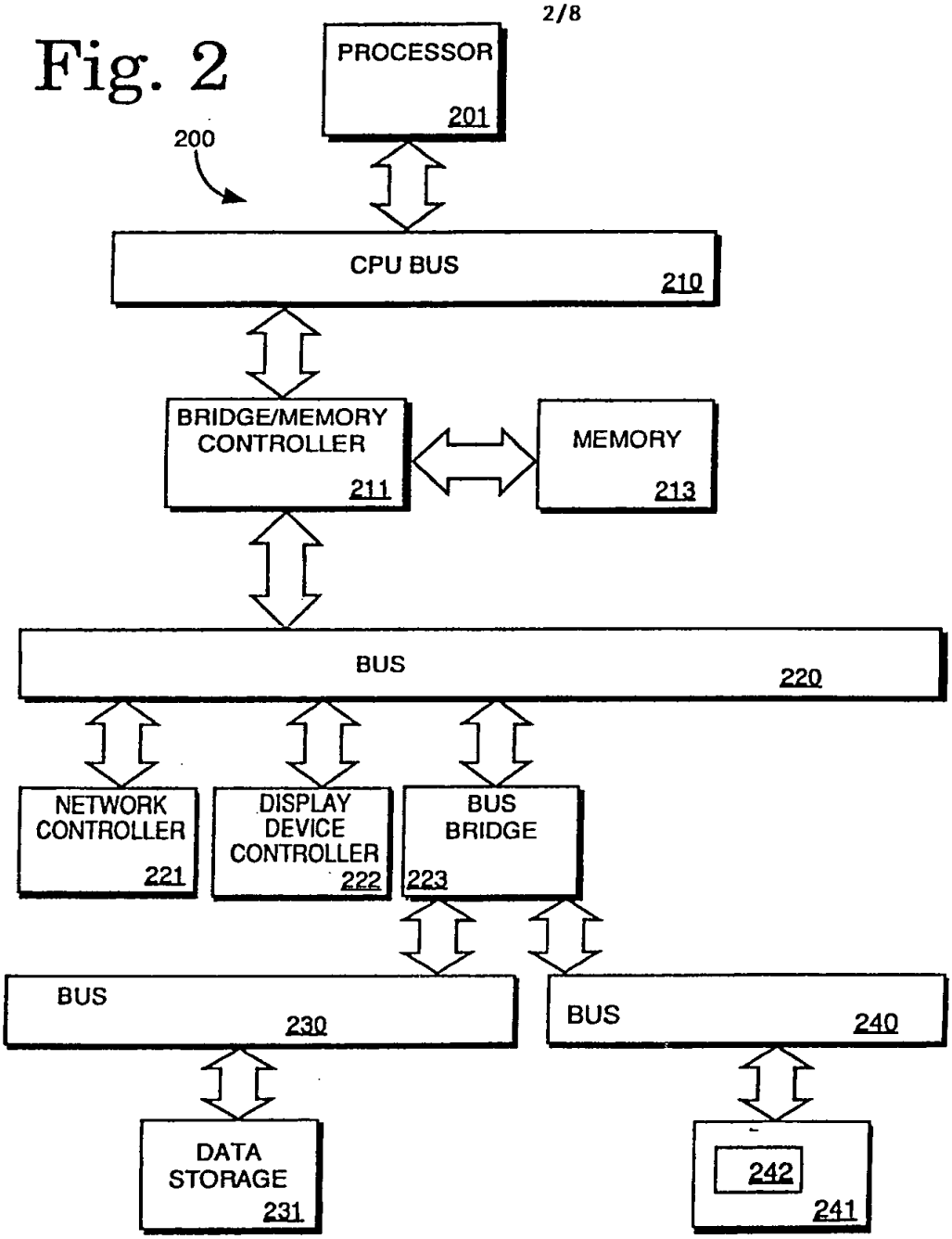


Fig. 2


PROCESSOR
201
200
CPU BUS
210
BRIDGE/MEMORY CONTROLLER
211
MEMORY
213
BUS
220
NETWORK CONTROLLER
221
DISPLAY DEVICE CONTROLLER
222
BUS BRIDGE
223
BUS
230
BUS
240
DATA STORAGE
231
242
241

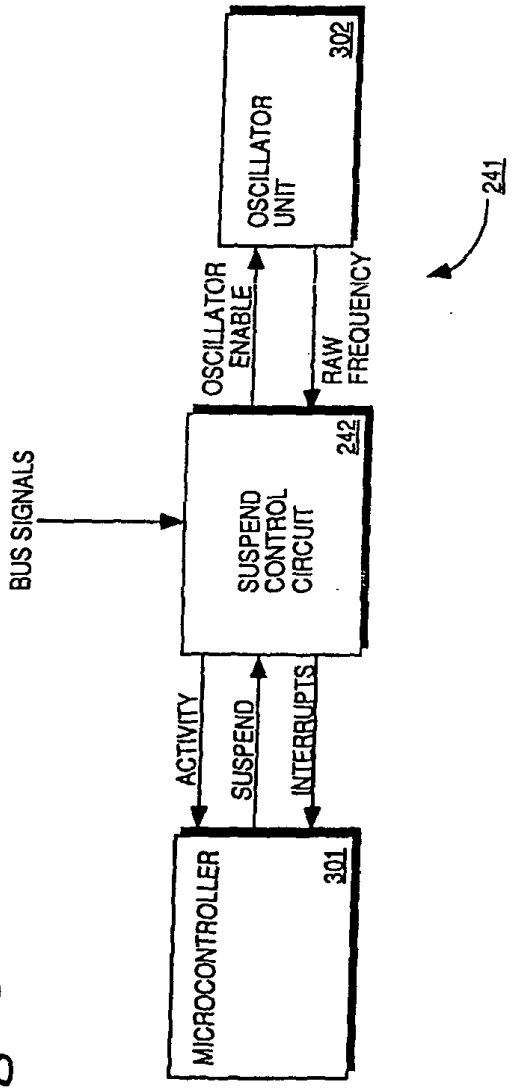

OSCILLATOR UNIT
302
241
OSCILLATOR ENABLE
RAW FREQUENCY
BUS SIGNALS
SUSPEND CONTROL CIRCUIT
242
ACTIVITY
SUSPEND
INTERRUPTS
MICROCONTROLLER
301

Fig. 3

Fig. 4

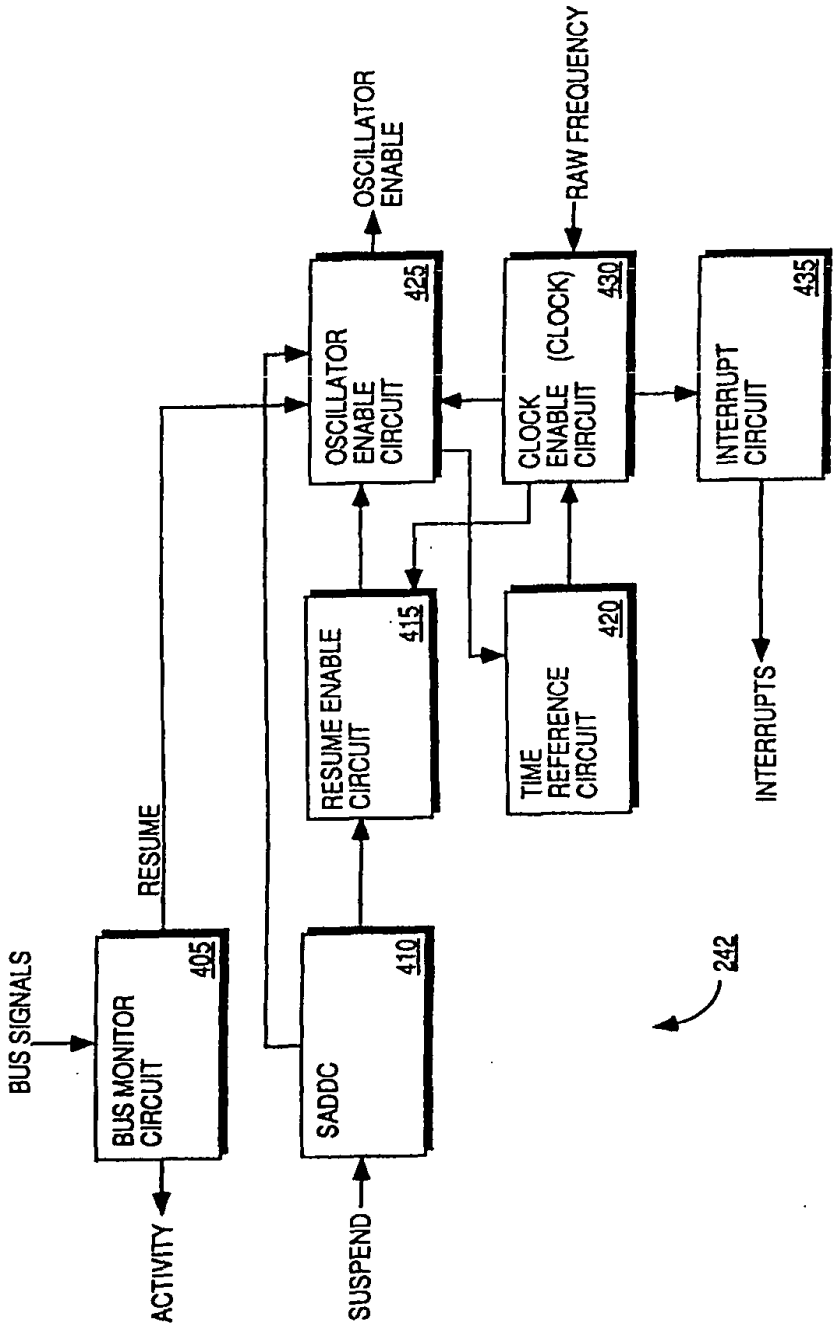

BUS SIGNALS
BUS MONITOR CIRCUIT
405
ACTIVITY
RESUME
SADDC
410
SUSPEND
RESUME ENABLE CIRCUIT
415
OSCILLATOR ENABLE CIRCUIT
425
OSCILLATOR ENABLE
TIME REFERENCE CIRCUIT
420
CLOCK ENABLE (CLOCK) CIRCUIT
430
RAW FREQUENCY
INTERRUPT CIRCUIT
435
INTERRUPTS
242

Fig. 5

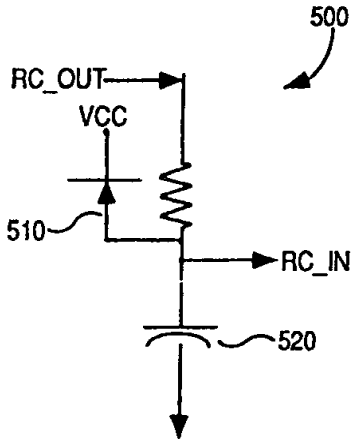


Fig. 6

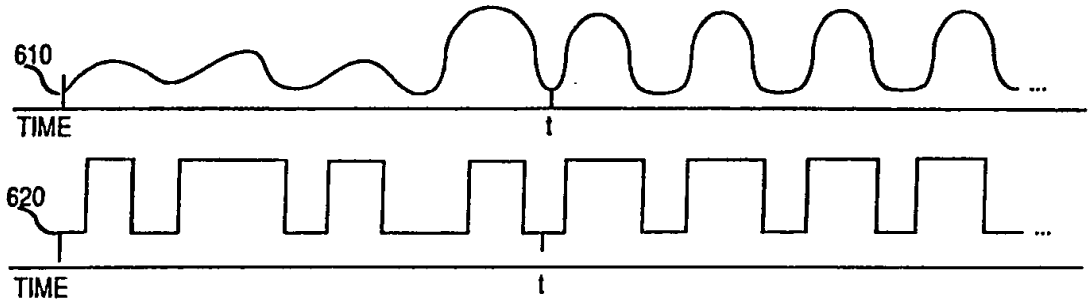


Fig. 7

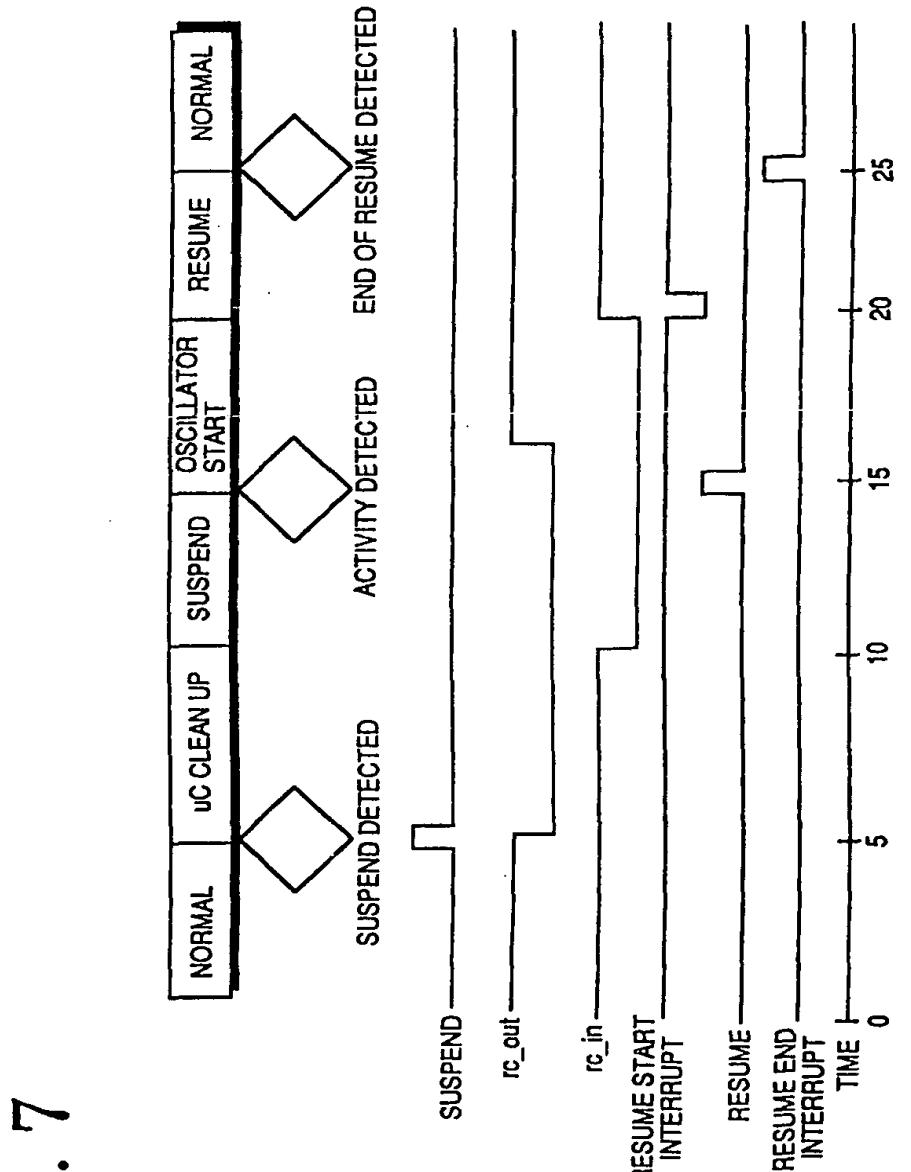
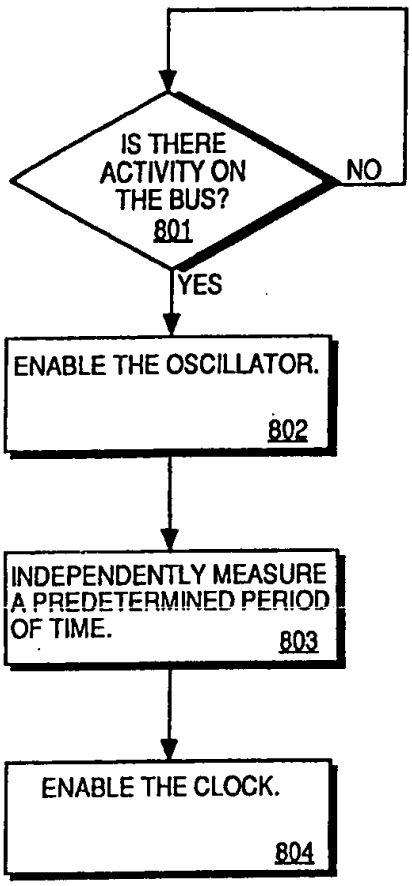

NORMAL
uC CLEAN UP
SUSPEND
OSCILLATOR START
RESUME
NORMAL
SUSPEND DETECTED
ACTIVITY DETECTED
END OF RESUME DETECTED
SUSPEND
rc_out
rc_in
RESUME START INTERRUPT
RESUME
RESUME END INTERRUPT
TIME
0
5
10
15
20
25

Fig. 8


IS THERE ACTIVITY ON THE BUS?
801
NO
YES
ENABLE THE OSCILLATOR.
802
INDEPENDENTLY MEASURE A PREDETERMINED PERIOD OF TIME.
803
ENABLE THE CLOCK.
804

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/21246

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 1/32
US CL : 395/750; 364/707
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/750, 750.01, 750.03, 750.04; 364/707

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Maya, APS
Manag? power, sav? power, bus or buses, time reference circuit, time(5a)independent, oscillator or oscillators, suspend state.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,502,689 A (PETERSON ET AL.) 26 March 1996, see figs. 1-8; col. 5, lines 61-67; col. 6-10.	1-23
X,P	US 5,628,020 A (O'BRIEN) 06 May 1997, see figs. 1-3; col. 3-4.	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 MARCH 1998	13 APR 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Ayaz Sheikh Telephone No. (703) 305-9648

Form PCT/ISA/210 (second sheet)(July 1992)*